

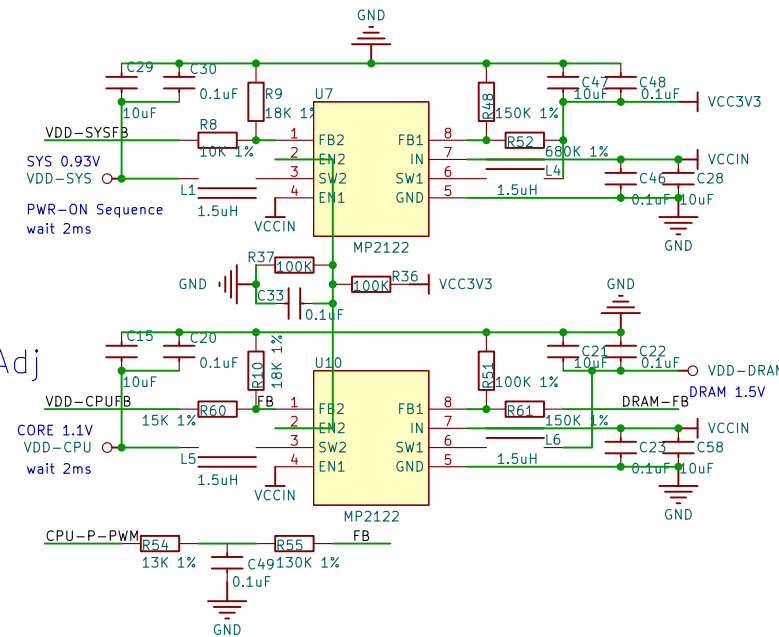
串口	
PB8	0
PB9	0
PC0	2
PC1	2
PD21	1
PD22	1

I2C	
PE16	3
PE17	3
PG13	0
PG12	0

PWM	
PB5	0
PB6	1
LCD_PWM	2 LED

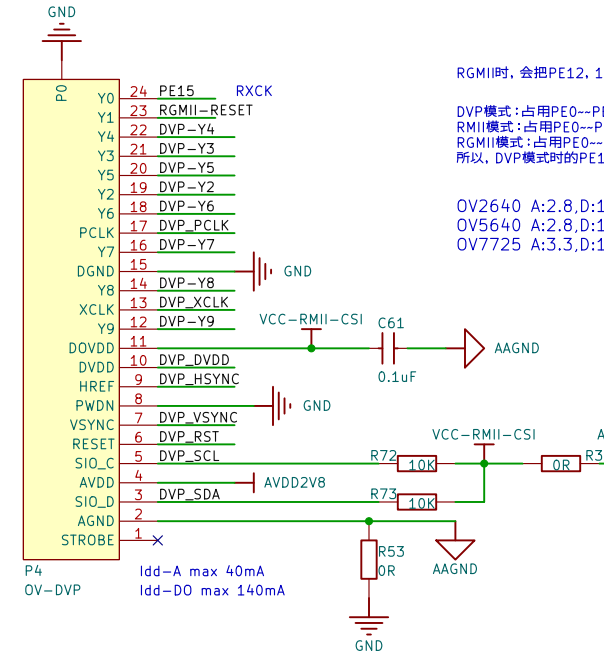
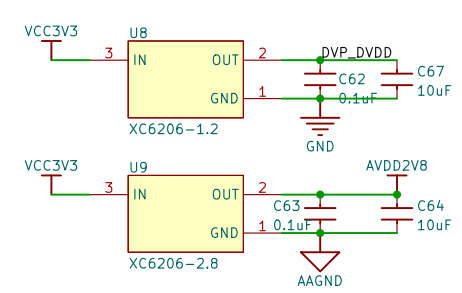
SYS

CPU-Adj



DVP(with TWI2)/RMII/RGMII

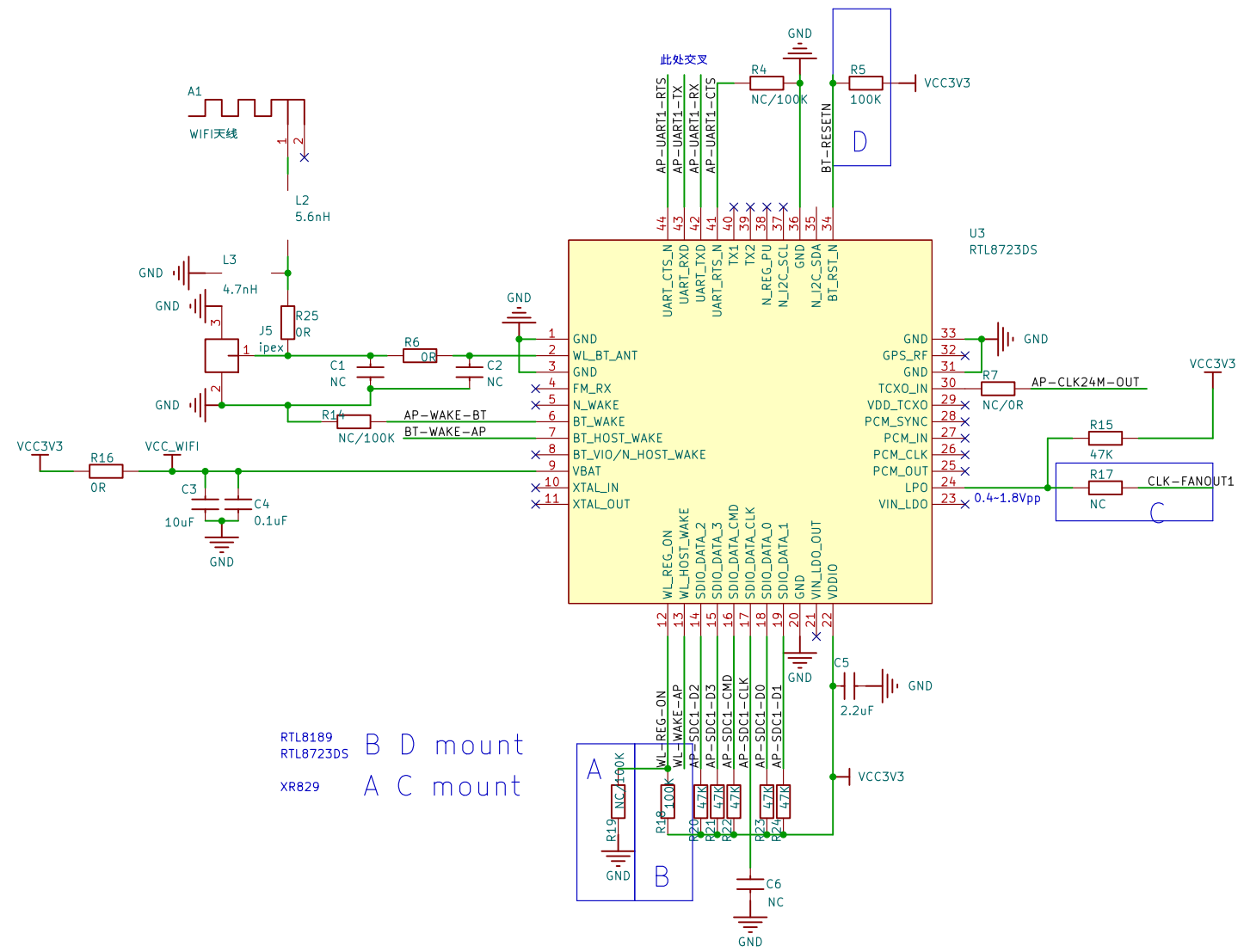
DVP_HSYNC	PE0
DVP_VSYNC	PE1
DVP_PCLK	PE2
DVP-Y2	PE4
DVP-Y3	PE5
DVP-Y4	PE6
DVP-Y5	PE7
DVP-Y6	PE8
DVP-Y7	PE9
DVP-Y8	PE10
DVP-Y9	PE11
DVP_XCLK	PE3
DVP_SCL	PE12
DVP_SDA	PE13
DVP_RST	PE14



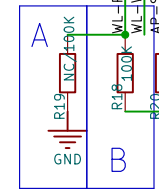
RGMII时, 会把PE12, 13的twi2占用
 DVP模式: 占用PE0--PE14
 RMII模式: 占用PE0--PE10
 RGMII模式: 占用PE0--PE15, 外加一个RST控制IO
 所以, DVP模式时的PE12, PE13 (TWI2) 为专用IO

OV2640 A:2.8,D:1.2,I0:1.8/2.8/3.3
 OV5640 A:2.8,D:1.5,I0:1.8/2.8
 OV7725 A:3.3,D:1.8,I0:2.8/3.3

DSI/LVDS + CTP(twi3)



RTL8189 B D mount
 RTL8723DS
 XR829 A C mount



此处交叉

